## AMENDMENTS TO THE SPECIFICATION

Please replace the original title with the following:

**-- CCD IMAGE DETECTOR AND METHOD OF OPERATING A CCD AS AN IMAGE DETECTOR --.**

Please replace the abstract with the following new abstract:

-- A CCD image detector includes an image area array, a storage area array, a buffer area array, and a readout shift register, all of which being controlled by a timing controller through separate and independent clock signals. The timing controller controls the transfer of the charge content of an image from the image area array to the storage area array and batch transfers of the charge content of the image from the storage area array to the buffer area array in bands of adjacent rows of gates. Between such batch transfers of bands, the timing controller controls the transfer of the charge content of the band stored in the buffer area array to the readout shift register one row of gates at a time at a slow rate to permit the charge content of each row to be shifted out from the readout register. The batch transfers of bands has the effect of minimizing slow rate transfers from the storage area array which reduces the impact of degraded charge transfer efficiency on performance of the image detector. --.

Please rewrite paragraph 0016 as follows:

-- The CCD 42 further includes a buffer area 52 of an array of rows of gates, each gate of the buffer area array 52 being operative to store a charge content. The rows of gates of the buffer area 52 are operative concurrently by a third clock signal CLK3 to transfer in parallel the charge contents of the gates of each row to the gates of an adjacent row in the predetermined direction through the buffer area 52. The buffer area array of rows 52 is disposed in the CCD [~~detector~~] 42 such that a first row 54 of the storage area array of rows 46 is adjacent a last row 56 of the buffer area array of rows 52 to accommodate a transfer in parallel of the charge contents of the gates of the first row 54 of the storage area 46 to the gates of the last row 56 of the buffer area 52, wherein the storage and buffer areas are operative by the second and third clock signals, CLK2 and CLK3, respectively, to transfer the charge contents of the rows of the storage area array 46 to rows of the buffer area array 52. The size of the buffer area array 52 being optimized

substantially by number of rows in relation to the rows of the image area array for charge transfer efficiency performance. This optimization process will be more fully described by way of example herein below. --.

Please rewrite paragraph 0017 as follows:

-- Further included as part of the CCD 42 is a readout or horizontal register 58 of a row of gates, each gate of the readout register 58 being operative to store a charge content. The readout register 58 is disposed in the CCD [~~detector~~] 42 such that a first row 60 of the buffer area array of rows 52 is adjacent the row of the readout register 58 to accommodate a transfer in parallel of the charge contents of the gates of the last row 60 of the buffer area 52 to the gates of the readout register 58 as controlled solely by the third clock signal CLK3. The row of gates of the readout register 58 being operative concurrently by a fourth clock signal CLK4 to transfer serially the charge contents of the gates thereof through the register 58 in a predetermined direction to an output signal line 62 of the detector 40. --.

Please rewrite paragraph 0021 as follows:

-- The timing controller 64 may be embodied as a hardwired circuit using interconnected logic gates operated in a predetermined combinational and/or sequential manner, or as a programmable read only memory or gate array, or as a programmed microcontroller, for example. In either case, the logic flow of the timing controller 64 defines a method of operating the CCD 42 which may be described in connection with steps of a flow chart. An exemplary logic flow chart for the operation of the CCD [~~detector~~] 42 for a band read out application is shown in Figures 3A-3B. As described herein above, for a band readout application, the image and storage areas 44 and 46, respectively, are divided into a set or plurality of bands wherein each band includes a predetermined number of adjacent rows of charge content. Referring to Figures 3A-3B, in the initial step or block 80, the CCD 42 is purged of charge content utilizing all clock signals. While the present embodiment includes a purging step, it is understood that in some applications, no separate purge cycle prior to the step of integration or charge collection is used. Rather, a frame transfer may define the step of integration without a charge purge. --.

Please rewrite paragraph 0025 as follows:

-- An exemplary logic flow chart for the operation of the CCD [~~detector~~] 42 for a frame image read out application is shown in Figure 4. As described herein above, for a frame image readout application, the image and storage/buffer areas 44 and 46/52, respectively, are divided into a plurality of adjacent bands wherein each band includes a predetermined number of adjacent rows of charge content. If the buffer area 52 is optimized substantially for a frame image of 512 rows, for example, by taking the square root of the number of rows and rounding it up to the nearest integer. The number of rows in the buffer area will be 23 and for optimization purposes, the predetermined number or rows in each adjacent band of the frame image will be set at 23 rows. Thus, the image and storage/buffer areas may be divided into 23 bands, 22 of which containing 23 adjacent rows and 1 of which containing 6 adjacent rows, to render a total of 512 rows or the entire frame image. --.